KYOCERA AVX THIN FILM TECHNOLOGIES

KYOCERA AVX Components Corporation
One AVX Boulevard
Fountain Inn, S.C. 29644 USA

KYOCERA AVX THIN FILM TECHNOLOGIES

TABLE OF CONTENTS

Introduction to KYOCERA AVX Thin Film Technologies 2

Typical Substrate Properties, Sputtered and Electroplated Materials, Wafer Construction 3

Resistor Technology, Capacitor Materials 4

Inductors 5

Typical Metalizations 6

Typical Hybrid Circuit Features, Enhanced Vias® 7

Hybrid Circuit Design Guidelines 9

General Design Guidelines 10

RF Testing Capability, Modeling 11

Assemblies 13

Inspection Methods, General Ordering Information 14

KYOCERA AVX THIN FILM TECHNOLOGIES

INTRODUCTION TO KYOCERA AVX THIN FILM TECHNOLOGIES

Engineered Thin Film Solutions

KYOCERA AVX is pleased to introduce Myrtle Beach, South Carolina Thin Film product capabilities. We offer a wide range of custom hybrid circuits, along with thin film resistors, capacitors, inductors, as well as lumped element and distributed filters, integrated passives, modules, heat sinks, and other unique thin film microelectronic solutions.

Design, Fabrication, Assembly, and RF Testing Services

Myrtle Beach Thin Film Products

KYOCERA AVX Thin Film operations, located in Myrtle Beach, SC, offers an array of thin film passives including resistor networks, capacitors, inductors, along with integrated passive LC and RC filters and modules. Six inch (150 mm) wafer technology offers the designer build-to-print or custom designs based on Ansys 3D HFSS modeling from for a broad spectrum of frequencies. These products will meet the most demanding requirements of circuit miniaturizations, tolerance and signal integrity applications.

Our Thin Film operations also provides a broad spectrum of high reliability metalized hybrid circuits. Designers can select from a wide variety of substrate materials, as well as vias, crossovers and bridges. Whether built to print or designed to a performance specification, the experienced engineering staff is available to assist in optimizing your product. In addition, two-sided assembly and RF testing are value-added services.

Combined Capabilities

- Design: Modeling (Ansys, Sonnet), Simulation (Genesys, ADS), and CAD (dxf, dwg)
- Substrates: 1 inch square to 6 inch round (150 mm) wafers
- Typical materials: Alumina, Aluminum Nitride, Beryllium Oxide, Silicon, (N, P, and N+), Quartz, Glass, Sapphire, Ferrites and Titanates
- Metallizations:
  - Sputtered: Al, Au, Cr, Cu, Ni(V), Pt, TaN, Ti and TiW
  - Plated: Electrolytic Cu, Ni, Au; Electroless Au
- Resistors: High Ohmic SiCr and TaN resistors in laser trimmable designs
- Capacitors: Si02, SiON and BCB dielectrics
- Inductors: Multilevel and multiturn copper and gold inductors
- Passivation Materials: SiON, Si_3N_4, BCB and polyimide
- Vias: Sputtered, enhanced plated, filled and castellations
- I/Os: BGA, LGA, edge wrap, through via and wire or ribbon bond
- Machining:
  - CO2 cutting, drilling, and scribing
  - Diamond-saw dicing
  - Back grinding and polishing
- Assembly:
  - High precision 0201 or larger pick and place
  - Attachment via wire or ribbon bonding, BGA, LGA or surface mount reflow
  - Encapsulation
- Testing:
  - MIL-STD-105D level II sampling
  - MIL-STD-883 100% visual inspection
  - Capacitance, insulation resistance and resistivity
  - RF testing to 40 GHz

Primary Markets and Applications

- Military, Aerospace and Space:
  - RF and Microwave filters
  - Precision resistors
  - MOS capacitors
  - Circulators, Splitters
  - Specialized modules
- Medical and Instrumentation:
  - Precision resistor networks and arrays
  - In-circuit trimmed designs
  - Telemetry filters
  - Miniature circuits and assemblies
- Broadband infrastructure:
  - Laser diode mounts and heat sinks
  - Optoelectronic converters
  - RF and DC fan-outs
- Instrumentation:
  - Ultra-precision reference capacitors and resistors
- Solar:
  - Interposers and heat sinks

KYOCERA AVX THIN FILM TECHNOLOGIES

TYPICAL SUBSTRATE PROPERTIES, SPUTTERED AND ELECTROPLATED MATERIALS, WAFER CONSTRUCTION

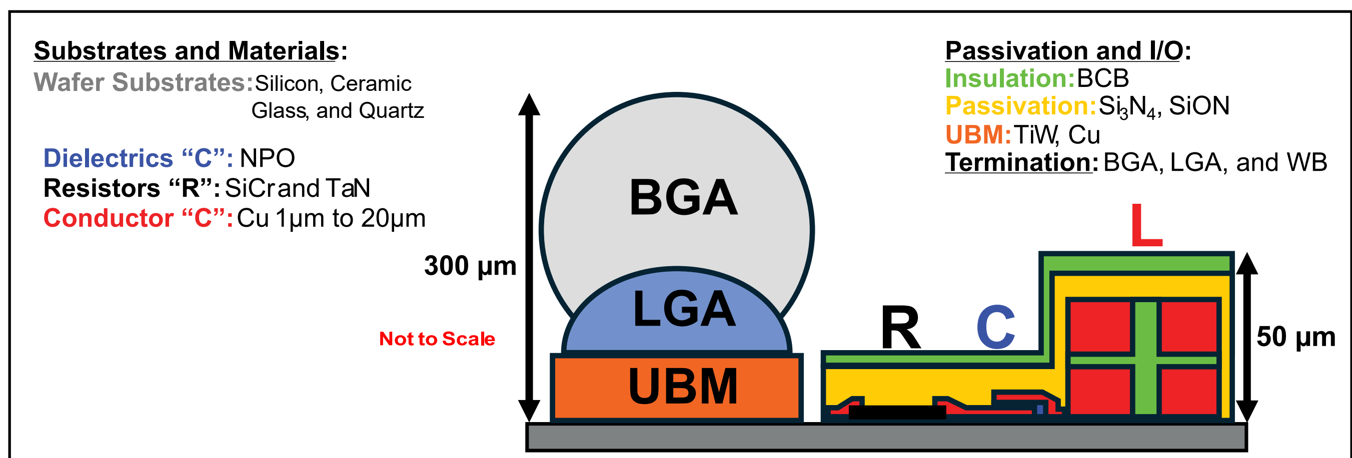
Typical Substrate Properties

Properties Nominal	Al_2O_3 99.6%	Al_2O_3 96.0%	Fused Silica	BeO 99.5%	AIN	Glass Borosilicate	P-Silicon Boron Doped	N++ Silicon Arsenic
Thickness Range (mil)	4-50	10-50	4-25	10-60	10-60	20	2-25	4-25
As Fired (Surface finish)	3µ"	No	No	6µ"	No	10 Å	N/A	
Lapped (Surfance finish) µ"	<20	No	No	<20	<20	N/A		
Polished (Surfance finish) µ"	<2	<4	<1	<3	<3	<.04	<.04	
Dielectric Constant @ 10 GHz	9.8	9.6	3.8	6.6	8.7	5.1	N/A	
Loss Tangent @ 10 GHz	0.0002	0.0002	0.0001	0.0003	0.001	0.003	N/A	
CTE (PPM/°C)	6.7	8.2	0.5	7.5	4.5	3.2	2.6	
Thermal Conductivity (W/mK)	25.5	24.7	1.38	280	170	1.16	150	
Volume Resistivity (ohm-cm)	10^14	10^14	10^14	10^14	10^13	10^13	15	0.002
Dielectric Strength (KV/mm)	8.7	8.3	100	14	>10	N/A		

Sputtered and Electroplated Materials

Materials	Sputtered	Comments
Al	150-40000 Å	Typical 2000 – 15000
Au	1000-65000 Å	Typical 3000 – 10000
Cr	150-5000 Å	Typical 600
Cu	2000-65000 Å	N/A
Ni(V)	500-10000 Å	N/A
Pt	100-4000 Å	Typical 2500
TaN	300-1500 Å	Barrier Layer
Ti	500-5000 Å	Typical 600
TiW	300-1500 Å	Typical 500
Plated Material	**Electrolytic µm and (µin)**	**Electroless µm and (µin)**
Au	0.5-25 (20-1000)	1-3 (40-120)
Cu	5 – 150 (200-6000)	N/A
Ni	1.25 – 5 (50-200)	N/A

Wafer Construction Overview

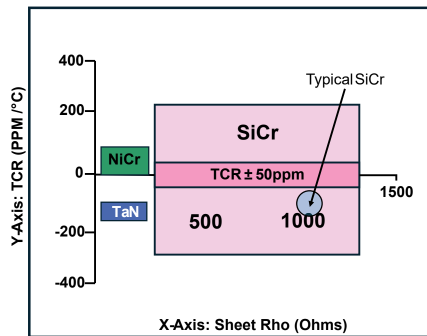


KYOCERA AVX THIN FILM TECHNOLOGIES

RESISTOR TECHNOLOGY, CAPACITOR MATERIALS

Resistor Technology

Thin Film Resistors	SiCr	TaN
Process	High Ohmic, High Voltage, Ultra-stable	High process temperature (no diffusion); Resistance to harsh environment
Typical Sheet Resistivity (ohm/sq)	500-1300	10-100
TCR (ppm/°C -25 to 125°C))	±50; ±100; ±250	-100 to -150
Stability (Change after 1000 hours @ 125°C)	0.2%	0.2%
Maximum Stabilization Temperature (°C)	550	450
Recommended Device Environment	Ambient Atmosphere	Amibient Atmosphere
Maximum Device Processing Temperature	Up to 1 hr. @ 400 °C	Up to 1/2 hr. @ 350 °C
Tolerance (the greater of)	0.5% or 0.1Ω	0.5% or 0.1Ω

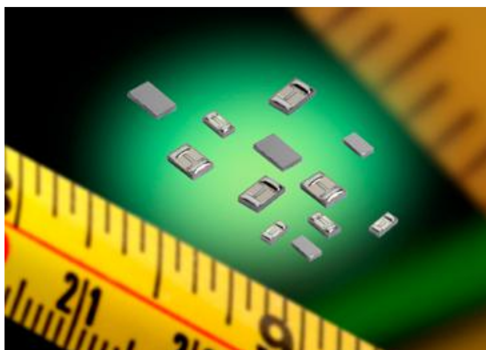


Resistor Materials

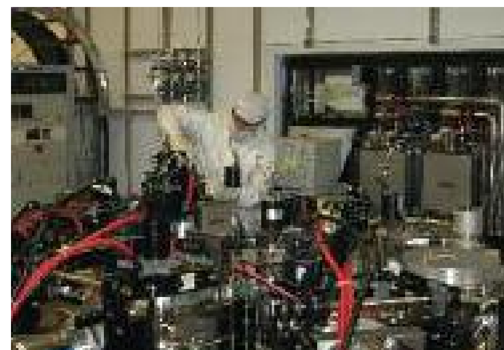
Precision Resistors

Capacitor Material Typical Values

Material	SiON	SiO_2	BCB	PI
pF/mm2 Typical	55	35	25	30
Range	1-500 pF	1-500 pF	1-50 pF	0.5-10 pF
Tolerance; NOTE: value dependent	±5%	±2.5%	±20%	±20%
Stability	±60 ppm/°C	±30 ppm/°C	±42 ppm/°C	±100 ppm/°C
BDV (v/μm)	600	1000	300	200
DF	≤ 0.1%	≤ 0.1%	≤ 0.1%	≤ 0.2%
Performance	K 5.8; TCC 60	K 4.0; TCC 30	K 2.7; TCC 42	K 3.3; TCC



Precision Capacitors



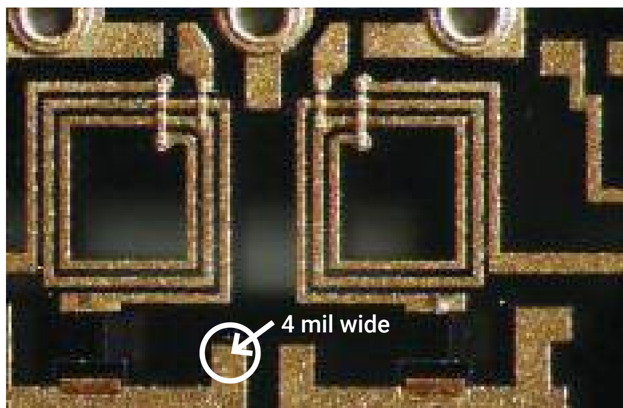
Multi-target Sputter System

KYOCERA AVX THIN FILM TECHNOLOGIES

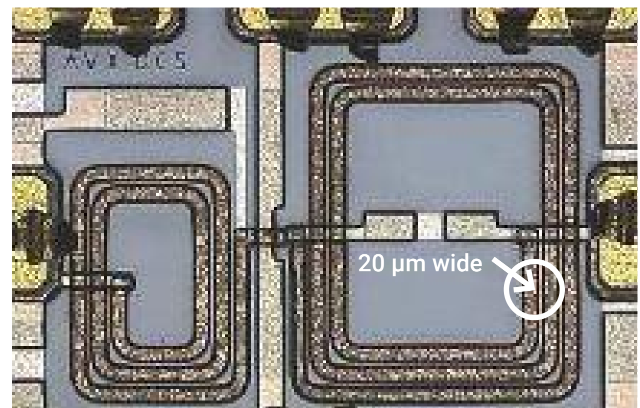
INDUCTORS

Typical values range from 0.1 - 45 nH. The coil material consists of patterned plated copper or gold on a sputtered seed layer. The preferred substrates for hybrid assembly construction are supplied either polished or as-fired. Typical dimensions for hybrid substrate designs (in micrometers) are: 25 µm wide, 20 µm spacing at < 5 µm thick. 50 µm wide, 46 µm spacing at < 10 µm. thick, 125 µm wide, 100 µm spacing, 12.5 – 75 µm thick. See design summary below:

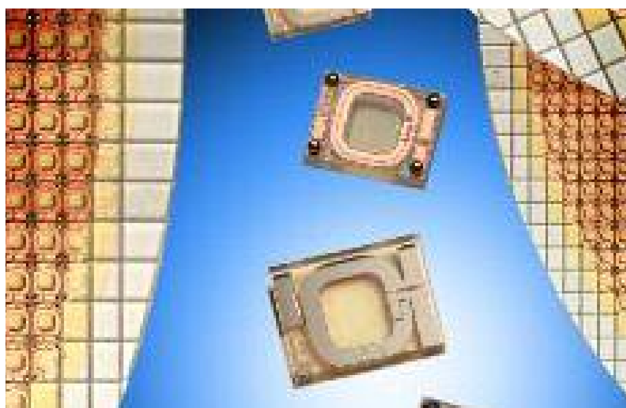
Construction Platform	Width (µm)	Spacing (µm)	Height (µm)
Hybrid	25	20	5
	50	46	> 10
	125	100	75
Wafer	> 10	> 10	Max 20*
*BCB Dielectric Separator layers 5-10 µm			



Hybrid Inductor



Wafer Inductor



Precision Inductors

Inspection

TYPICAL METALIZATIONS

Typical Metalizations

Typical Hybrid Metalizations	Application	Attachment Method	Metalization/ Resistor Layers	Typical Value
1. TaN –TiW – Ni(V)* – Au	RF/Microwave circuits: attenuators, loads and DC biasing networks. Hybrids with resistors and spiral inductors. End products: Power supplies, couplers, splitters, filters, amplifiers, SAW devices, laser diode mounts and others.	Epoxy Wire Bonding	TaN 10 to 200 ohms/sq. TiW 300 to 1000 Å NiV 1000 to 2000 Å Au 20 to 300 µin	50 500 1500 150"
2. TiW – Ni(V)* – Au	Same as 1. – without resistors	Epoxy Wire Bonding	TiW 300 to 1000 Å NiV 1000 to 2000 Å Au 20 to 300 µin	500 1500 150
3. TaN –TiW – Au – Ni – Au	Same as 1. – When repeated soldering is required for repairs	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TaN 10 to 200 ohms/sq. TiW 300 to 1000 Å Au 20 to 300 µin Ni 50 to 150 µin Au 20 to 200 µin	50 500 20 min. 50 min. 150
4. TiW – Cu – Ni* – Au	High Power/Low Loss RF and Power Supply	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TiW 300 to 1000 Å Cu 200 to 2000 µin Ni 50 to 150 µin Au 20 to 200 µin	500 500 50 min. 150 min.
5. TiW – Au – Cu – Ni* – Au	High Power/Low Loss RF and Power Supply	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TiW 300 to 1000 Å Au 3000 to 5000 Å Cu 200 to 2000 µin Ni 50 to 150 µin Au 20 to 200 µin	500 3000 min. 500 50 min. 150 min.
6. TaN – TiW – Au Cu – Ni* – Au	High Power/Low Loss RF and Power Supply with Resistors	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TaN 10 to 200 ohms/sq. TiW 300 to 1000 Å Au 3000 to 5000 Å Cu 200 to 2000 µin Ni 50 to 150 µin Au 20 to 200 µin	50 500 3000 min. 500 35 min. 150 min.

* Optional

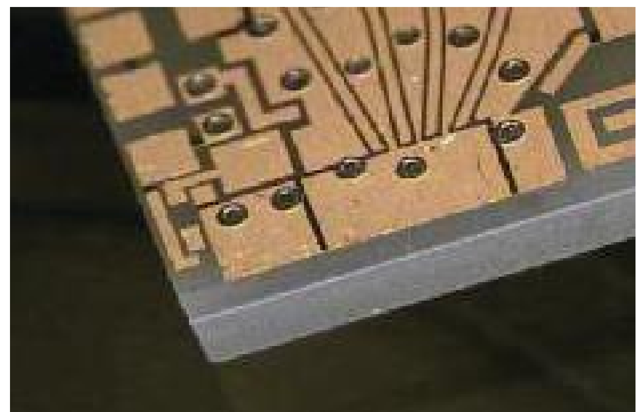
Other metalizations available upon request.

TYPICAL HYBRID CIRCUIT FEATURES, ENHANCED VIAS®

Typical Hybrid Circuit Features

Circuit Feature	Specifications
Conductors:	Lines and spaces width ≥ .0005 inches
Resistors:	Tolerances ≥ 1%, Contact factory for tighter tolerances
Via Holes:	Conventional or Enhanced Vias®
Crossovers:	With Polyimide over conductor lines
Wraparounds:	Edge patterning
Solder Dam:	Polyimide, Ni Oxide and others

Enhanced Via®

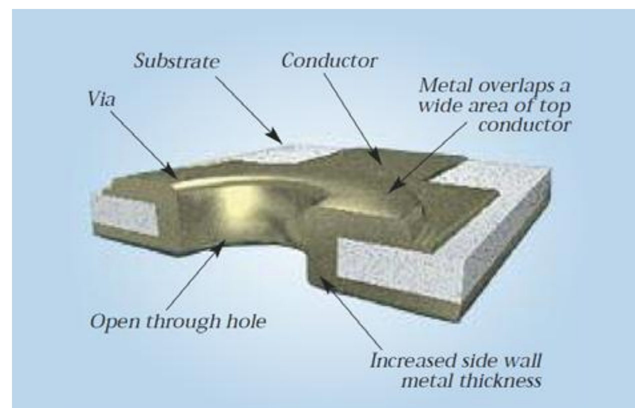


Ni Oxide Solder Dam Stop

Enhanced Vias®

Designed for Improved Performance:

- Low contact resistance due to the increased metal thickness
- Uniform metallic connection to top and bottom surfaces ensures highest reliability and minimum contact resistance
- Increased overlap area improves robustness
- Pure plated Cu Au for epoxy and eutectic die-bond attachments
- Optional Ni barrier for solder attachments
- No ceramic filler materials
- Minimal occurrence of closed voids
- No entrapment of liquids and gases
- Through hole provides ability to visually inspect via after mounting to carrier
- Via plugging options available to prevent epoxy or solder wicking

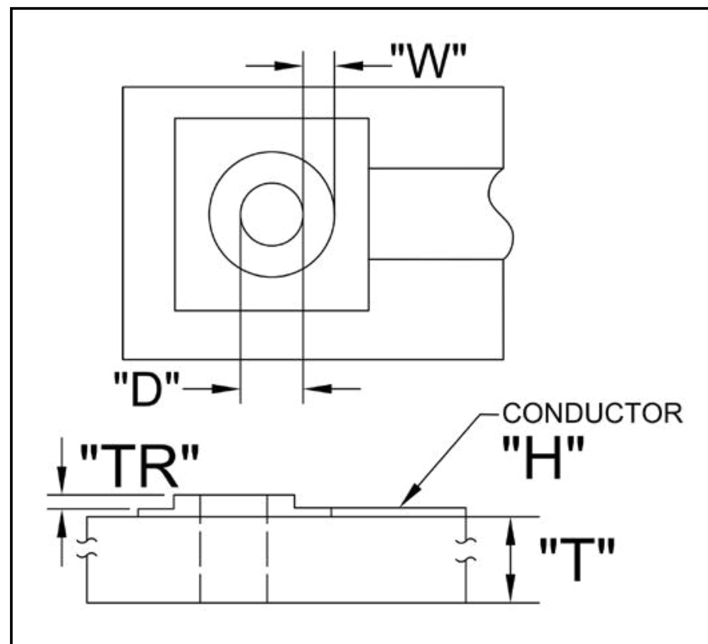


Enhanced Via®

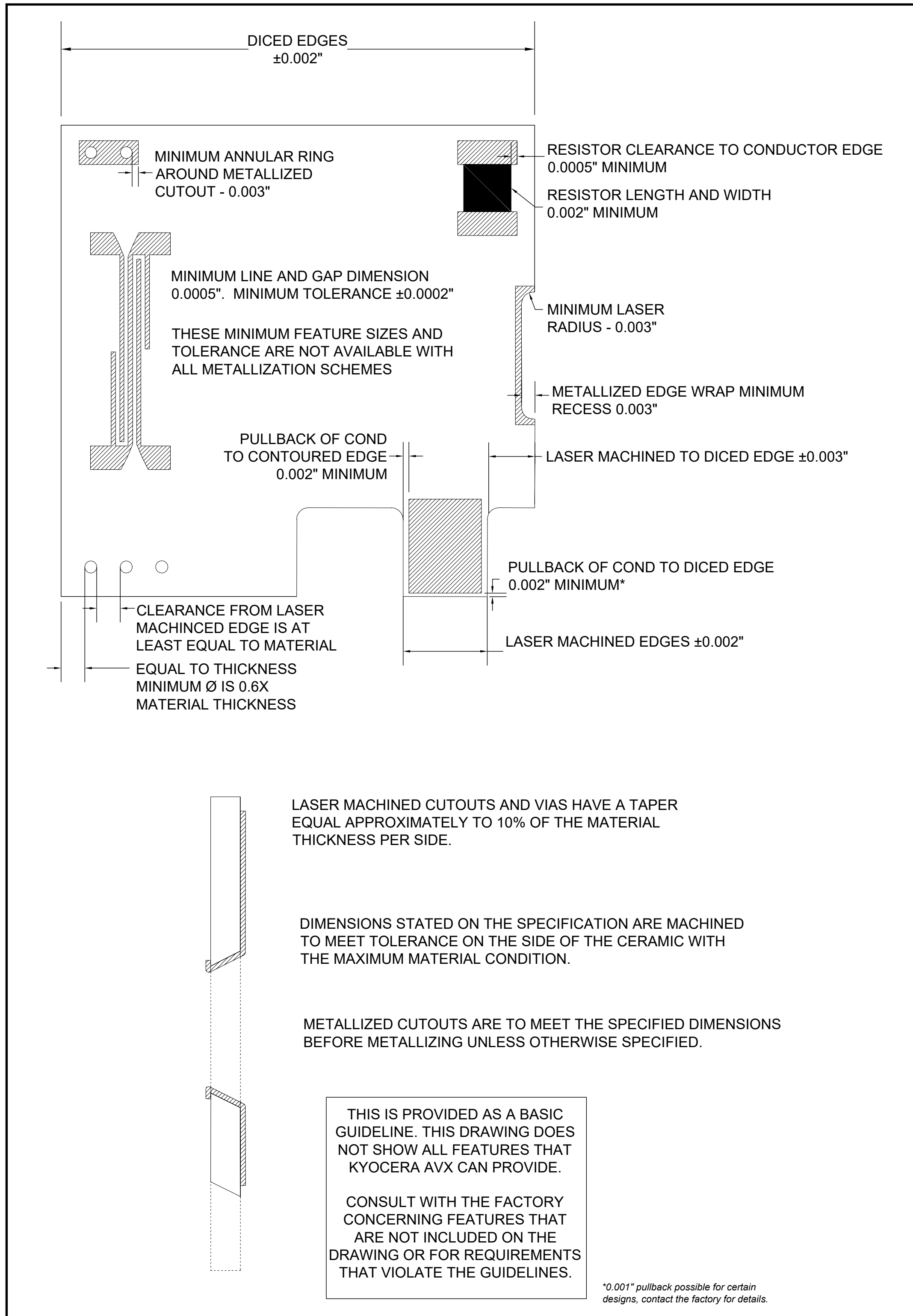
TYPICAL HYBRID CIRCUIT FEATURES, ENHANCED VIAS®

Design Guidelines for Enhanced Vias®

Parameter	Symbol	Limits/ Recommendations
Hole Diameter	D	Minimum: 0.6 X T Nominal: >=1 X T
Rim Width	W	Minimum: 0.002" Nominal: 0.005"– 0.025"
Rim Thickness	TR	Per request
Nominal DC Resistivity (mΩ) (T&D in mils, TR&H in μ")	$\frac{318 \times T}{D \times (TR+H)}$	



Hybrid Circuit Design Guidelines



GENERAL DESIGN GUIDELINES

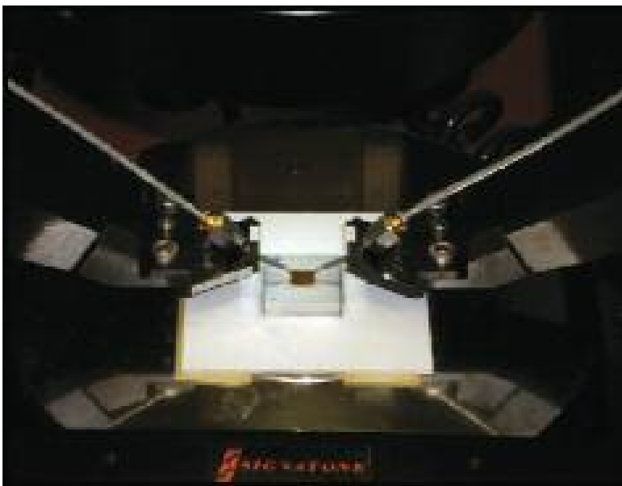
General Design Guidelines

		Hybrid (inches)	Wafer (µm)
Conductors	Minimum Line Width / Minimum Space Width	.0005	10
	Line Width Tolerance	.0002 Standard .0001 Select	±3
	Space Tolerance	.0002 Standard .0001 Select	±3
	Minimum Pad Size Around Via (D = hole diameter)	.006 + D	±10
Resistors	Minimum Tolerance	0.5% or 0.1Ω	.5%
	Minimum Spacing Between Resistors	.002	4
	Minimum Length and / or Width	.002	4
	Pre Trim Designed Value	-20%	-20%
	Nominal Sheet Resistance (ohms/sq) Preferred Sheet Resistance (ohms/sq)	20 – 100 50 or 100	20-100 or 500-1500 Ohms/sq
Teminations	Minimum Pad Size (Wire Bond)	.003 x .003	75 x 75
Metalized Holes (Via's)	Minimum Aspect Ratio (Hole diameter: Substrate thickness)	0.6:1	N/A
	Minimum Tolerance	.002	
	Minimum Distance from Hole Circumference To Edge (T = substrate thickness) or adjacent hole circumference	T	
	Minimum True Center Tolerance	.001	
Substrates	Minimum Thickness Tolerance	±.005	±10
	Minimum Length / Width Tolerance	.001	N/A
	Surface Finish (Microinch – CLA not available in all materials)	.2 – 10	.001
	Minimum Camber (Polished only) Typical Camber – Polished Typical Camber – As Fired	.0002 / inch .0005 / inch .002 / inch	10 across 150 millimeters

RF TESTING CAPABILITY, MODELING

RF Testing Capability

KYOCERA AVX RF test capabilities include full two (2) and four (4) port test measurements using a vector network analyzer. Compensation up to the device under test (DUT) is typically performed with a custom calibration (short-open-load- through - SOLT) method to acheive the most accurate measurements possible. When necessary, other methodologies are employed. In addition, specialized test structures are designed and fabricated in-house for specific requirements of the DUT. The typical frequency measurement range is from 50 MHz to 40 GHz with optional testing capability to 67 GHz. An automated in-line data analysis system enables a quick pass-fail sorting process to a frequency-defined template, or provides serialized complete S-Parameter data for the customer.

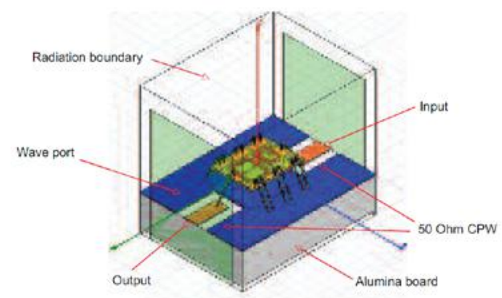


Modeling

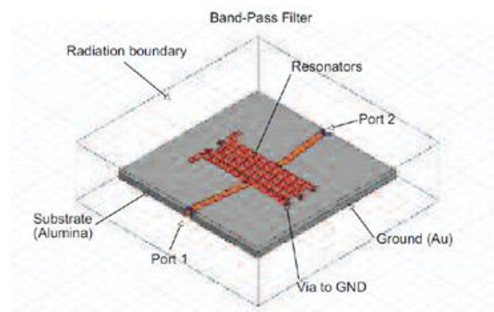
KYOCERA AVX models utilize the latest versions of Ansys Electronics including HFSS for full 3D geometry software. is method uses finite element analysis of the models using tetra h e d rons to obtain a 3D design. The combination of the 3D design and selection of appropriate dielectric materials and metalization is critical to the final design. The close correlation between the design, models and materials, offers the advantage of virtual processing. All designs are validated with measurements during the fabrication build process.

Complete Radiation Environmental Simulation

Lumped - Element Topology

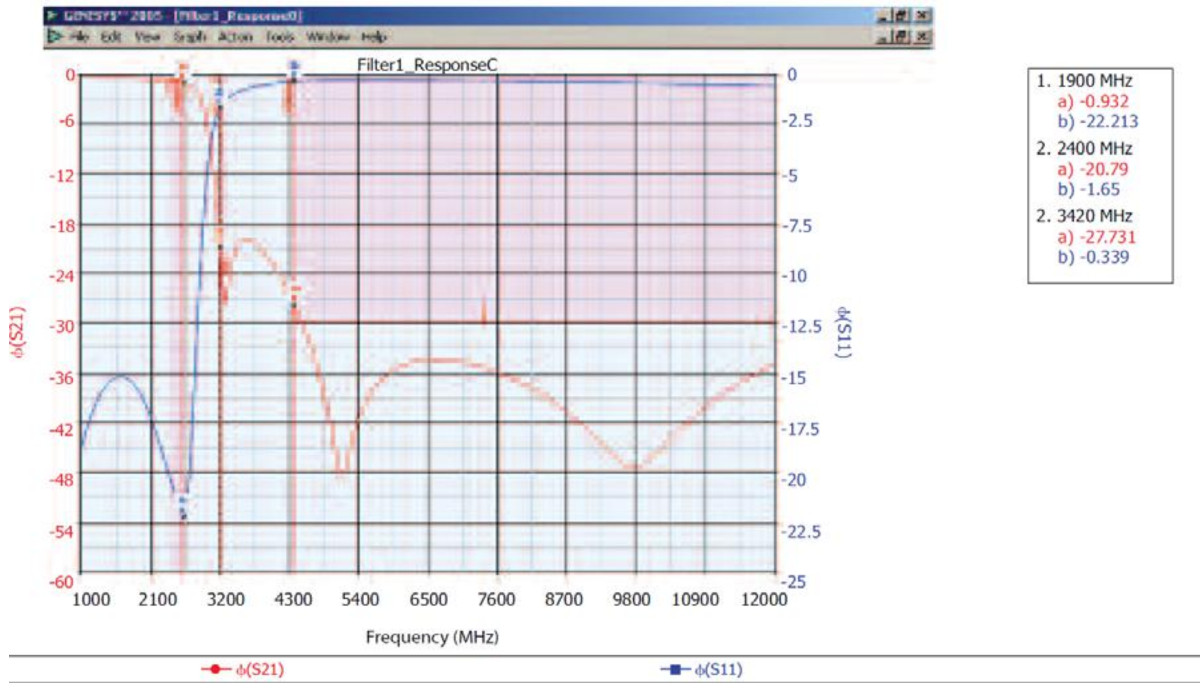


Distributed Band-Pass Topology

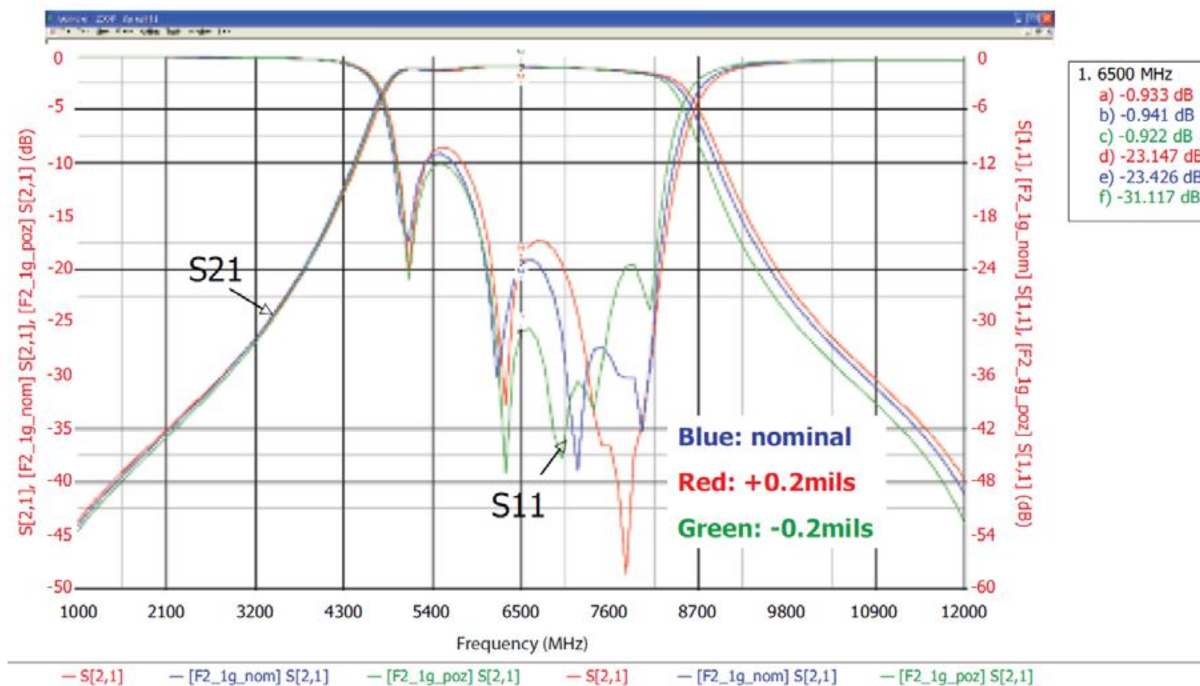


RF TESTING CAPABILITY, MODELING

HFSS Simulation Lumped-Element Topology



S-Parameters as Simulated by HFSS (Process line-width sensitivity)



ASSEMBLIES

Assemblies

KYOCERA AVX assembly begins with high-precision pick-and-place of surface mount devices 0201 and larger including CSPs, µBGAs, flipchips, ultra-fine-pitch [.012" (0.3 mm) lead pitch] QFPs and irregularly shaped components requiring ± .0005" (± .0125 mm)placement accuracy.

Die attach includes:

- Adhesive die attach – electrically / thermally conductive or electrically insulating epoxies
- Solder Die attach – lead or lead free for example, Sn63/Pb, 95Pb-5Sn,80Au-20Sn,88Pb,SAC305
- Wire/Ribbon Bonding – automated ball and wedge bonding, ribbon/ wedge bonding and gold stud bumping.

Encapsulation:

- Includes polymers, hermetic and non-hermetic structures and inhouse fabricated ceramic enclosures.

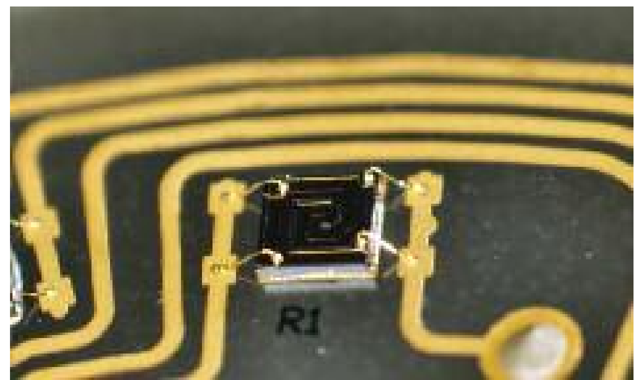
Additional assembly processes:

- Screen and stencil printing
- Automated dispensing (>7 mil diameter dots and lines)
- Parallel gap welding
- Solder tinning
- Via plugging (gold paste/epoxies)
- Solder mask application

Pick and Place

Pick from Waffle Pack

0201 Soldering



Epoxy LED Attachment and Wire Bonding

INSPECTION METHODS, GENERAL ORDERING INFORMATION

Two-sided assembly (top)

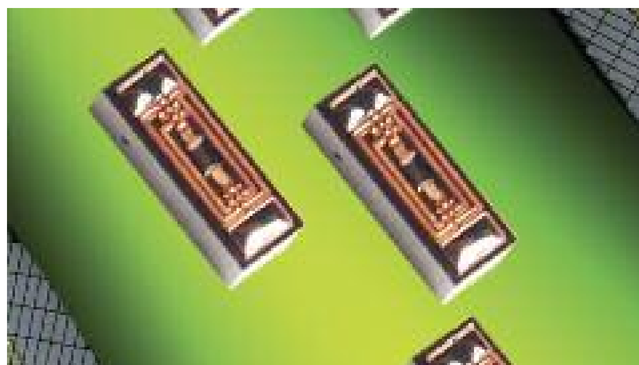
Two-sided assembly (bottom)

Inspection Methods

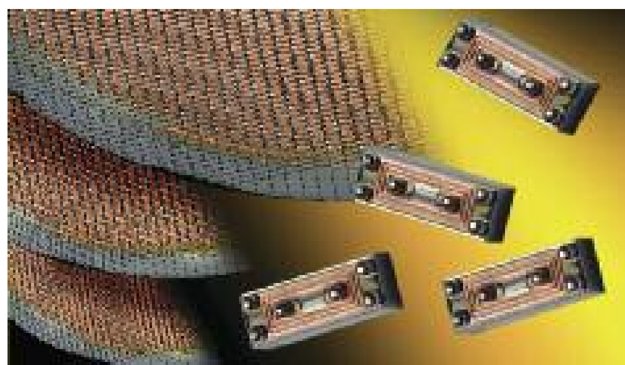
Visual	100%	Per MIL-STD-883, method 2032 Class H or K (10X microscope min.)
Dimensional	AQL	Pattern features: Microscope; Substrate: Micrometer and calipers
Resistors	AQL	2 or 4 Point Probe
Adhesion	AQL	Tape pull test; die shear
Other	Customer Specified	

General Ordering Information

Substrates	Type, surface finish, dimensions and tolerances.
Resistsive Films	Type, nominal resistivity, tolerance after heat treatment. Heat treatment temperature and time.
Conductive Films	Type, thickness and tolerance.
General	Specifications and acceptance criteria.
Artwork	Dimensioned Drawings, DXF, DWG, Gerber or GDS Formats.
Processing	Temperatures, bonding/soldering methods and environment.



LGA 0402 Filters



BGA 0603 Filters

NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250

NOTICE: Specifications are subject to change without notice. Contact your nearest KYOCERA AVX Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable, but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should not assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all applications.

WWW.KYOCERA-AVX.COM