



TECHNICAL INFORMATION

SURFACE MOUNT TANTALUM CAPACITOR APPLICATIONS INFORMATION

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Abstract:

Surface mount tantalum capacitors, like all electronic components, impose restrictions on pad (or land) design and solder processing to achieve minimum defects. Proper pad designs and the reasons behind those designs are discussed and solder process constraints are outlined for wave and reflow soldering.

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Introduction

Surface mount tantalum capacitors, like all electronic components, impose restrictions on pad (or land) design and solder processing to achieve minimum defects. Proper pad designs and the reasons behind those designs are discussed and solder process constraints are outlined for wave and reflow soldering.

Pad Designs

Proper pad design is essential for reflow soldering because only molten solder surface tension holds the part in place. That surface tension can work for or against high yields and is controlled by pad design and solder mass present. Pad designs must take into account component size and dimensional tolerance, metallization areas and solder paste thickness. Solder paste thickness is not a limiting factor of soldering coplanar parts like tantalum capacitors but is a major factor with non-coplanar parts like integrated circuits (ICs). Thicker solder paste laydown is needed to fill gaps that are left when the IC leads are not in the same plane, minimizing missing solder joints on those devices. Solder surface tension is the defect generating force for coplanar parts so as solder mass is increased to minimize defects of IC leads, passive component defects rise. A practical limit for solder paste wet laydown is 10-12 mils with no solder bridging and minimum solder balls after reflow. When thicker wet laydowns are used, solder bridging between IC leads becomes a major source of defects and solder balls increase which can also bridge across closely spaced conductors.

When tantalum capacitors are reflow soldered, interaction between the molten solder surface tension, component metallization and substrate pad determine the magnitude of defect and counter defect generating forces. Minimum soldering defects requires maximum counter forces and minimum defect generating forces. This occurs with minimum solder but non-coplanar parts dictate the solder paste wet laydown thickness so a compromise is needed to compensate for the larger solder mass. Early experiments with multilayer ceramic capacitors (MLCs) showed a direct correlation between defects

such as tombstoning or standing up, drawbridging, rotation, solderable termination and pad size. There are minimum induced defects when the pad width matches the component solderable termination width.

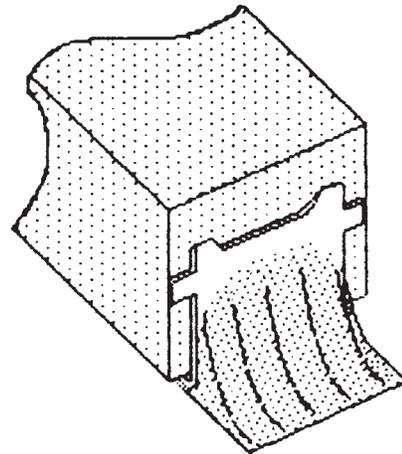


Figure 1. Pad Width and Solderable Termination Width

Induced defects are also at a minimum when the amount the termination overlaps the pad equals the amount that the pad extends beyond the termination face. Another limitation that determines pad length is the termination length. Defects (tombstones, etc.) are minimized by the adhesion of molten solder to the opposite termination so the overlap must equal the solderable termination length under the part, now the pad is approximately twice the solderable bottom side length.

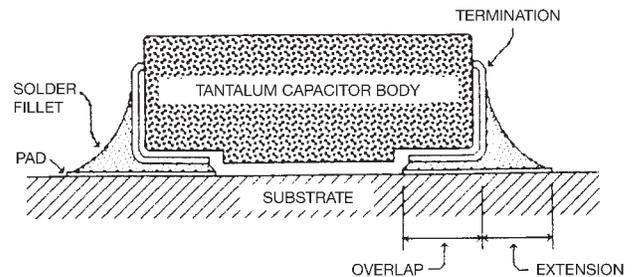


Figure 2. Tantalum Capacitor Showing Overlap and Extension

Defects such as tombstones with short parts and drawbridges with longer parts are caused by an imbalance of forces. Component rotation is eliminated by matching pad width to that of the solderable termination but minimizing the other defects is not quite as easy. Defects are caused by excessive surface tension on the termination face and is countered by solder adhesion to the opposite termination bottom land. A quick fix of placing most of the pad under the part works when very little solder is used but when ICs are soldered at the same time, the capacitors will float and roll on a large dome of solder. In this case the components can now short to one another and exhibit increases in tombstone defects. Surface tension is required to hold parts in place and allow for inspection of the solder fillet. Changing the overlap to extension ratio (O/E) the other way by extending the pad well beyond the termination end increases the number of defects because now surface tension force is increased.

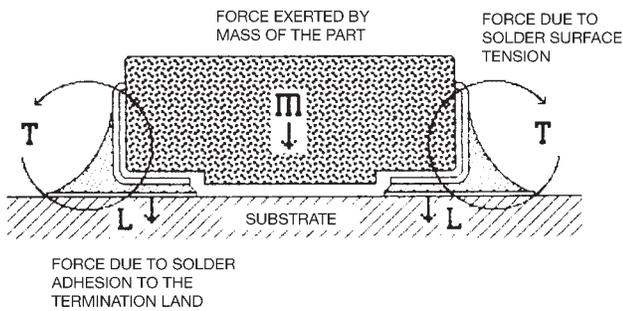


Figure 3. Forces Exerted by Molten Solder on the Terminations

Adhesion of molten solder to the termination face creates a rotational moment that tries to stand the component up, hence the name "Tombstone". That rotational moment is counteracted by a short moment arm formed by $1/2$ of the component length and its mass and another moment arm formed by the component's length and adhesion of solder to the bottom land of the opposite termination.

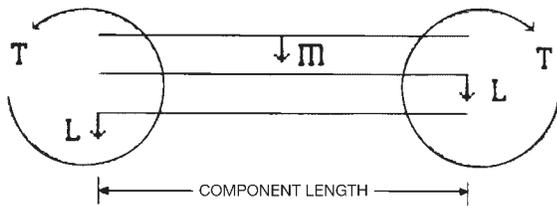


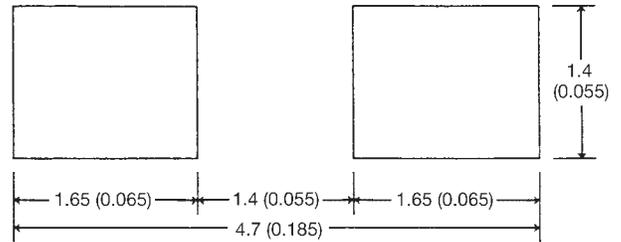
Figure 4. Defect and Counter Defect Forces

Longer, high mass components have few defects because of large counter defect forces while short parts are very susceptible to these forces so pad design is critical for the two small case sizes (A, B) and not as critical for the C and D sizes.

Pads for the C and D case sizes are identical to current IPC recommendations but the A and B pads are different. IPC pads for the A and B case sizes have excessive overlap and are too long. The A case size pads shown in Figure 5 have been used in production with a solder joint history in excess of 10 million and a defect rate in the low ppm range (<1). The B case pads are an extension of the A case pads, meeting the low defect criteria of $O/E \approx 1$ with solder paste wet laydown at 10-12 mils. Both C and D case size pads have $O/E \approx 1$.

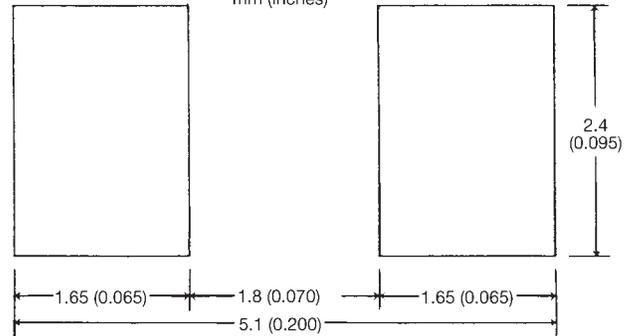
A CASE SIZE

mm (inches)



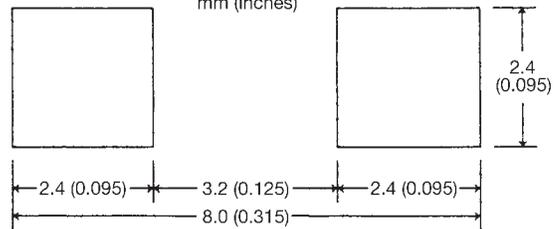
B CASE SIZE

mm (inches)



C CASE SIZE

mm (inches)



D CASE SIZE

mm (inches)

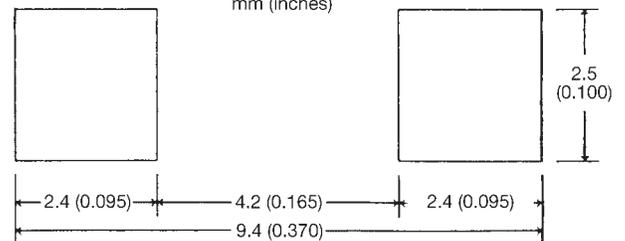


Figure 5. Tantalum Capacitor Reflow and Wave Soldering Pads

Soldering Tantalum Capacitors

Excessive exposure to soldering temperatures of electronic components impairs reliability. This is due in part to the acceleration of component wear out at elevated temperatures and extra internal mechanical stress from differences in the CTE (coefficient of thermal expansion) of materials used in the manufacture of those components. Every electronic component has these limitations which establish boundary conditions for the soldering process. Process limitations of tantalum capacitors are very similar to other epoxy resin molded components such as transistors, diodes and ICs. Each surface mount soldering process uses different heat transfer techniques which impose different soldering time and temperature limitations on the capacitors.

MATERIAL	CTE (ppm/°C)
Alloy 42	5.3
Alumina	≈7
Copper	17.6
Filled Epoxy (ϵT_g)	18-25
Nickel	15
Silver	19.6
Steel	15
Tantalum	6.5
Tin Lead Alloys	≈27

Table I. CTEs of Component Materials

Wave Soldering

Wave soldering uses the highest temperatures and heat transfer rates. High temperatures are used because the molten solder must supply the heat required to heat component land patterns to the solder liquidus temperature in addition to supplying solder for the fillet. Solder pot temperatures can be reduced when higher preheat temperatures are used but much of the installed equipment base has inadequate preheat. Figure 6 shows the allowable time and temperature ranges for wave soldering. Five seconds is the maximum dwell time for a single wave or total wave time in dual wave systems at 250°C but is extended to a maximum of 7.5 seconds at 230°C. There is a small band of extended temperatures and times when preheat is used where

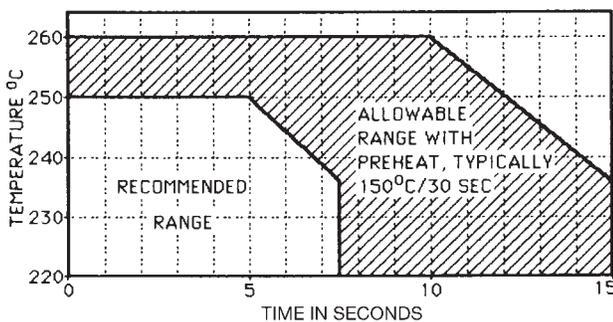


Figure 6. Wave Soldering Time and Temperature Combinations

the part can be used but they should be avoided if possible.

Vapor Phase Soldering

Vapor phase soldering has the second highest heat transfer rate from the condensing vapor latent heat of vaporization with peak temperatures limited to the fluid boiling point. There are two basic fluids used, high and low temperature, which determines component dwell time. The more common low temperature fluid has a safe range of 60 seconds and can be extended to 120 seconds if needed. Most vapor phase soldering dwell times are in this time range because of active device limitations.

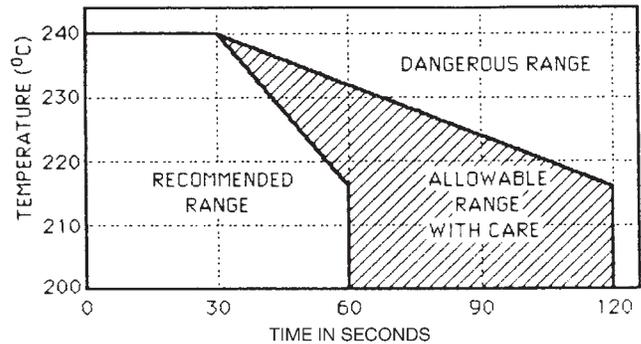


Figure 7. Vapor Phase and Convection Infrared Soldering Range of Time and Temperature

Infrared and Hot Belt Reflow Soldering

Hot belt reflow uses heat conduction through the substrate to reflow solder paste on component pads. Heater temperatures are above soldering temperatures and the thermal mass of the substrate will hold temperatures high so care must be taken to profile the substrate surface temperature to maintain process limits.

Infrared poses a different set of problems. IR soldering uses surface heating like vapor phase but the heat source is at higher temperatures than the substrate and component temperatures. Depending on the type or wave length of the IR source, there may be severe temperature gradients and possible component damage. Older IR systems are of the lamp type where emitter (lamp) temperatures are as high as 1200°C and have excessive amounts of visible light. These systems need nitrogen blankets to minimize visible PC board damage and discolorization but temperatures are still too high and there are color/temperature variations. The newer convection/IR reflow systems use lower emitter temperatures that are close to soldering temperatures. Emission wave lengths are such that there are no color selectivity problems with these systems as there is no visible

light. Additionally, component and substrate absorption characteristics are high allowing for more uniform heating.

Lamp IR systems have short peak wave lengths of emission which penetrate substrates and some components, heating their interior. This works well when heating small conductive substrates like alumina, but causes excessive internal temperatures

MATERIAL	.72 TO 3 MICRONS	3 TO 7 MICRONS
Ploymers	Absorptive	Absorptive
Ceramics	Transparent or Semi-Transparent	Absorptive
Metallic Elements	Reflective	Reflective
Expoxy Laminates	Semi-Transparent	Absorptive

Table II. Material Response to Radiated Infrared in insulating substrates like epoxy PC boards. Deep heating is best suited for sore muscles and joints and not for reflowing solder of epoxy laminate PC boards. Lamp IR systems should be reserved for soldering small hybrids or resistor/conductor firing on those same substrates.

With this in mind, temperature monitoring of capacitor surface is mandatory when lamp systems are used but component land temperatures are the

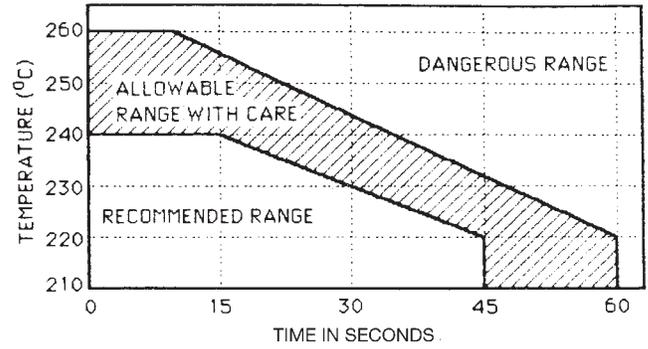


Figure 8. Infrared and Hot Belt Reflow Soldering Time/Temperature Combinations

control point for convection/IR systems. Figure 8 shows lamp IR and hot belt time/temperature combinations. Time is reduced from those shown for vapor phase soldering because of preheat times of lamp IR and hot belt reflow systems.

Each soldering technique has limits to avoid damage to the component but each allows proper solder fillet formation and good solder joint strength and while posing no limits other than is found for epoxy resin molded active components.

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